



BIRCK NANOTECHNOLOGY CENTER

National Nano Device Laboratories, Taiwan Seminar

Friday, December 1, 11:00 a.m. – 12:00 p.m.
Burton D. Morgan Center, Rm. 129

11-11:20 a.m.

**NDL Introduction: Beyond
More than Moore CMOS, Prof.**

**Wen-Kuan Yeh, Director of
National Nano Device
laboratories, Taiwan NDL**

(National Nano Device Laboratories) is an important place to cultivate high-level technology talents for semiconductor and nano techniques in Taiwan. It has become a national open nano device process test environment, and provided a unique open experiment research environment for comprehensive turnkey consignment services. As MOSFETs are scaled down to sub-10nm and below, power consumption is the major limitation to maintain device performance well.

11:00 am-11:20am)

11:20-11:35 a.m.

Development of Ge NW FETs

Dr. Yao-Jen Lee, NDL, Taiwan

Germanium is attractive for the future technology node application because of its two times higher electron mobility and 4 times higher hole mobility than that of Si counterpart. . The lower band gap of Ge also allows the supply voltage scalability to satisfy the post-Si CMOS era. However, the Ge MOSFET technology is facing several **serious** challenges, including fast n-type dopant diffusion, high junction leakage, EOT scaling, Dit reduction and enormous dislocation defects in the Ge epi-layer on Si substrates because of the large lattice mismatch to Si. Herein, we propose a feasible pathway to scale the Ge MOSFET technology by using a novel diamond-shaped Ge gate-all-around (GAA) nanowire (NW) FETs.

11:35-11:50a.m.

**Ge Devices with Ferroelectric
Hf_{1-x}Zr_xO Gate Stack Dr.**

Chun-Jung Su, NDL, Taiwan

Germanium (Ge) has been widely studied as a potential alternative channel material for sub-3nm technology node because of its high carrier mobility and process compatibility. In order to meet the requirements of steep subthreshold slope (SS) and low VDD operation for device scaling, the ferroelectric (FE) gate stack with negative capacitance (NC) effects has been proposed to tackle the fundamental thermionic limit of 60 mV/decade SS without causing loss to the drive current.